REMARKS

This is in response to the Office Action mailed September 25, 2001.

Claims 1 through 15 are pending in the application.

Claims 1 through 15 stand rejected. Applicant has amended claims 1 and 15 and respectfully requests reconsideration of the application as amended herein.

35 U.S.C. § 102 Anticipation Rejections

Anticipation Rejection Based on Admitted Prior Art

Claims 1, 4, 5, 7, 8 and 15 were rejected under 35 U.S.C. § 102(b) as being anticipated by the Admitted Prior Art by Applicant (Figs. 16-18).

A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference. *Verdegaal Brothers v. Union Oil Co. of California*, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). The identical invention must be shown in as complete detail as is contained in the claim. *Richardson v. Suzuki Motor Co.*, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).

Fig. 16 teaches a prior art semiconductor assembly, wherein a technique of face-down attachment of a semiconductor die 232 onto a semiconductor substrate 234 with an adhesive tape 236 has been utilized. With this technique, the semiconductor substrate 234 has an opening 238 therethrough with electrical connections 240 (shown as bond wires) extending through the opening 238 to connect the bond pads 242 on an active surface 262 of the semiconductor die 232 to the traces 244 on an active surface 250 of the semiconductor substrate 234. The adhesive tape 236 used in these assemblies **is generally narrow and does not extend proximate an edge 246 of the semiconductor die 232**. Further, the opening 238 is filled and the electrical connections 240 are covered with a glob top material 256 injected into the opening 238, as shown in FIG. 17. Also, as shown in FIG. 18, an encapsulant material 258 is molded over the semiconductor die 232.

In contrast to such prior art, Claim 1, recites, *inter alia*, "at least one adhesive tape interposed between and attaching said semiconductor die active surface and said semiconductor substrate first surface, wherein a width of said at least one adhesive tape extends at least **proximate an edge** of said at least one semiconductor die **to at least proximate an edge of said at least one semiconductor substrate opening**." (Emphasis added). Figs. 16-18 of Applicant's disclosure do not contain each and every element of independent Claim 1. Specifically, none of the prior art figures show an adhesive tape that extends at least proximate an edge of at least one semiconductor die to at least proximate an edge of at least one substrate opening.

Therefore, the prior art does not teach each and every element of independent Claim 1. Accordingly, Claim 1 is allowable. Claim 4-5 and 7-8 are each allowable as depending either directly or indirectly from independent Claim 1, which is allowable.

Similarly, independent Claim 15 recites, *inter alia*, "at least one adhesive tape interposed between and attaching said semiconductor die active surface and said semiconductor substrate first surface, wherein a width of said at least one adhesive tape extends at least proximate an edge of said at least one semiconductor die to at least proximate an edge of said at least one semiconductor substrate opening."

As discussed hereinabove, none of the prior art figures show an adhesive tape that extends at least proximate an edge of at least one semiconductor die to at least proximate an edge of at least one substrate opening. Accordingly, independent Claim 15 is allowable.

35 U.S.C. § 103 Obviousness Rejections

Obviousness Rejection Based on Admitted Prior Art in view of Admitted Prior Art

Claim 6 was rejected under 35 U.S.C. § 103(a) as being unpatentable over the Admitted Prior Art (Figs. 16-18) in view of the Admitted Prior Art (Fig. 15).

After carefully considering the cited prior art, the rejections, and the Examiner's comments, Applicant respectfully traverses the obviousness rejection hereinbelow.

Applicant further submits that to establish a *prima facie* case of obviousness under 35 U.S.C. § 103 three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Third, the cited prior art reference must teach or suggest all of the claim limitations. Furthermore, the suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on Applicant's disclosure.

The prior art teachings of Figs. 16-18 of Applicant's disclosure are discussed hereinabove. In contrast to such, drawing Fig. 15 of Applicant's disclosure shows an exemplary COB assembly 200 comprising a semiconductor die 202 back-bonded with an adhesive layer 204 to a semiconductor substrate 206. The semiconductor die 202 is in electrical communication with the semiconductor substrate 206 through electrical elements extending between bond pads 208 on the semiconductor die 202 and traces 212 on the semiconductor substrate 206. The electrical elements are TAB connections 216. TAB connectors 216 (generally metal leads carried on an insulating tape, such as a polyimide) are attached to each bond pad 208 on the semiconductor die 202 and to a corresponding lead or trace 212 on the semiconductor substrate 206.

Applicant submits that there is no motivation to make the proposed combination. Applicant respectfully asserts that the only way one might find the present claims obvious under 35 U.S.C. § 103 is to engage in an impermissible hindsight reconstruction of the claimed invention from the Applicant's disclosure. Applicant submits that there must be some teaching, suggestion or motivation in the art, and not in Applicant's disclosure, supporting the Examiner's combination of references in the prior art. *See In re Fine*, 5 U.S.P.Q.2d 1596, 1599-1600 (Fed. Cir. 1988) ("One cannot use hindsight reconstruction to pick and choose among isolated disclosures in the prior art to deprecate the claimed invention"); *Uniroyal v. Rudkin-Wiley*, 5 U.S.P.Q.2d 1434, 1438 (Fed. Cir. 1988) (something in prior art as a whole must suggest

desirability of combination). That a prior art device could be modified to produce the claimed device does not justify an obviousness rejection unless the prior art suggested the modifications desirability. *In re Gordon*, 221 U.S.P.Q. 1125 (Fed. Cir. 1984).

Concerning Claim 6, it is asserted that one of ordinary skill in the art would have recognized that the TAB and bond wire are both considered to be an art recognized functional equivalent for providing the electrical interconnection." However, in order to rely on equivalence as a rationale supporting an obviousness rejection, the equivalency must be recognized in the prior art, and cannot be based on applicant's disclosure or the mere fact that the components at issue are functional or mechanical equivalents. *In re Ruff*, 118 U.S.P.Q. 340 (CCPA 1958).

Additionally, the prior art teachings fail to teach or suggest all of the claim limitations. Specifically, amended independent Claim 1, from which Claim 6 indirectly depends, recites, *inter alia,* "at least one adhesive tape interposed between and attaching said semiconductor die active surface and said semiconductor substrate first surface, wherein a width of said at least one adhesive tape extends at least proximate an edge of said at least one semiconductor die to at least proximate an edge of said at least one semiconductor substrate opening." None of the prior art figures teach or suggest an adhesive tape that extends at least proximate an edge of at least one semiconductor die to at least proximate an edge of at least one substrate opening. Therefore, Claim 6 is allowable as none of the prior art illustrations taken alone or in combination teach or suggest all of the claim limitations.

Obviousness Rejection Based on Admitted Prior Art in view of Yaguchi et al.

Claims 2, 3, and 9 through 14 were rejected under 35 U.S.C. § 103(a) as being unpatentable over the Admitted Prior Art (Fig. 18) in view of Yaguchi et al ("Yaguchi"). (WO 97/01865).

After carefully considering the cited prior art, the rejections, and the Examiner's comments, Applicant respectfully traverses the obviousness rejection hereinbelow.

The Admitted Prior Art teachings have been discussed above. Yaguchi teaches various configurations of CSP-type semiconductor devices. Further, Yaguchi suggests that insulating tape pieces may be pressed against the internal lead 3 for wire bonding and resin sealing. (Pg. 20, lines 15-26). In addition, Yaguchi teaches that "it is preferable to decrease the area of the tape from the viewpoint of reliability" because it easily absorbs water and is easily peeled in a package. (Pg. 20, lines 19-22).

Yaguchi fails to teach or suggest all of the claim limitations. In contrast to the teachings of Yaguchi, independent Claim 1 recites, *inter alia*, "a width of said at least one adhesive tape extends at least proximate an edge of said at least one semiconductor die." Yaguchi does not teach or suggest that an adhesive tape extends at least proximate an edge of at least one semiconductor die. Neither does any combination of Applicant's admitted prior art and Yaguchi teach or suggest that an adhesive tape extends at least proximate an edge of the at least one semiconductor die. Accordingly, claims 2, 3, and 9-14 are each allowable as depending directly or indirectly from independent Claim 1.

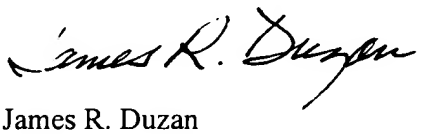
Further, there is no motivation to combine the Admitted Prior Art with Yaguchi, because Yaguchi teaches away from the Admitted Prior Art. Also, it is respectfully submitted that consideration of Yaguchi in its entirety teaches away from any combination with the Admitted Prior Art, and vice versa. More specifically, Yaguchi teaches that use of an adhesive tape should be minimized due to reliability considerations, as discussed hereinabove. Therefore, the proposed modification to Yaguchi to extend the adhesive tape proximate an edge of said at least one semiconductor die conflicts with the teachings of Yaguchi.

In contrast to Yaguchi, The Admitted Prior Art does not suggest minimizing the area of adhesive tape due to reliability considerations. In addition, the Admitted Prior Art does not teach or suggest using sections of adhesive tape to reduce the adhesive tape area. In other words, both references fail to provide any motivation for the attempted combination. The Examiner is respectfully reminded that it "is improper to combine references where the references teach away from their combination." M.P.E.P. §2145(X)(D)(2) (citing *In re Grasselli*, 713 F.2d 731, 743,

218 U.S.P.Q. 769, 779 (Fed. Cir. 1983)). A prior art reference must be considered in its entirety, i.e., as a whole, including portions that would lead away from the claimed invention. *W.L. Gore & Associates, Inc. v. Garlock, Inc.*, 220 U.S.P.Q. 303 (Fed. Cir. 1983), *see also* MPEP § 2141.02.

Applicant submits that claims 1 through 15 are clearly allowable over the cited prior art. Applicant requests the allowance of claims 1 through 15 and the case passed for issue.

Respectfully submitted,



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Enclosure: Version with Markings to Show Changes Made

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APPENDIX A

VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE SPECIFICATION:

Please amend the title as follows:

TAPE ATTACHMENT CHIP-ON-BOARD ASSEMBLIES [AND METHODS OF FABRICATING THE SAME]

IN THE CLAIMS:

A marked-up version of each of the presently amended claims, highlighting the changes thereto, follows:

1. (Twice Amended) A semiconductor die assembly comprising:

a semiconductor substrate having a first surface and a second surface, wherein said semiconductor substrate includes at least one opening defined therethrough between said semiconductor substrate first surface and said semiconductor substrate second surface;

at least one semiconductor die having an active surface with at least one electrical connection area disposed on said semiconductor die active surface, said at least one semiconductor die oriented having said at least one electrical connection area substantially aligned with said at least one semiconductor substrate opening; and

at least one adhesive tape interposed between and attaching said semiconductor die active surface and said semiconductor substrate first surface, wherein a width of said at least one adhesive tape extends at least proximate an edge of said at least one semiconductor die to at least proximate an edge of said at least one semiconductor substrate opening.

15. (Twice Amended) A computer comprising:

at least one semiconductor die assembly, said semiconductor die assembly comprising:

a semiconductor substrate having a first surface and a second surface, wherein said semiconductor substrate includes at least one opening defined therethrough between said semiconductor substrate first surface and said semiconductor substrate second surface;

at least one semiconductor die having an active surface with at least one electrical connection area disposed on said semiconductor die active surface, said at least one semiconductor die oriented having said at least one electrical connection area substantially aligned with said at least one semiconductor substrate opening; and

at least one adhesive tape interposed between and attaching said semiconductor die active surface and said semiconductor substrate first surface, wherein a width of said at least one adhesive tape extends at least proximate an edge of said at least one semiconductor die to at least proximate an edge of said at least one semiconductor substrate opening.